

ABSTRACT

Methods and apparatus for halting the data strobes transmitted over a source synchronous link to enable the data stored in the data capture flip-flops in a source synchronous receiver to be scanned out for subsequent analysis. This allows for the evaluation of the captured data without placing additional components in the functional data path and, therefore, without increasing the latency of the transmission. To provide optimal timing margins the data and data strobe paths are logically and electrically matched. This includes routing the data and data strobe signals in close proximity from the transmitter to the receiver, and through the same logical and physical elements in the transmitter and receiver. This insures that any injected link noise is experienced common-mode. In addition, the data strobe signal is preferably driven at one-half of the period of the data signal so that the data strobe and data signals experience logical state transitions at the same time and at the same frequency. This insures maximally similar electrical modes on the communication link, further maximizing link margin.

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